IEEE DASC P1076.1 Working Group

http://www.eda.org/vhdl-ams/

Working Group Meeting
January 15, 2014

Ernst Christen
WG Chair
christen.1858@comcast.net

Agenda

- Call to order
- Approval of agenda
- Administrative issues
  - Minutes of December 11, 2013 meeting
  - Review of IEEE patent policy
- Project review and plans
- Next meeting
- AOB
- Adjourn

Administrative Issues

- Approval of minutes of WG meeting
  - Meeting of December 11, 2013, available at http://www.eda.org/vhdl-ams
- Review of IEEE patent policy
  - http://standards.ieee.org/board/pat/pat-slideset.pdf

Project Status

- Projects considered for this revision of the language

Project	Champion	Status	Importance
Baselined LRM	Alain Vachoux	Clauses 1-6 done	required
VHPI-AMS	David Smith	started	
1076.1.1 integration	David Smith	depends on LRM	high
Mandatory changes	Ernst Christen	depends on LRM	required
Frequency domain modeling	Ernst Christen	done, needs WG approval	low-medium
Mixed netlists	Ernst Christen	not started	low-medium
Table-driven modeling	Joachim Haase	needs validation of use model	medium-high
Vector/matrix operations	Zhichao Deng	about 80% done	medium-high
Partial differential equations	Vipin Ahuja	started	

Proposal

- **Project champions to prepare project plan for each project**
  - Goal
  - Exact status
  - Remaining work
  - Plan to complete work
    - Resources
    - Time line
- **Present plan at next WG meeting**
- **Reach consensus which projects to pursue**
  - By end of February 2014
- **Focus only on projects that are not postponed**

Baseline LRM (1)

- **Objective: Develop a baseline conditional FrameMaker source document including the P1076.1-2007 and the P1076-2008 standards**
- **Status**
  - Clauses 0(1)* to 9(11) have been converted and verified against original LRM documents
    - * P1076.1-2007 numbering(P1076-2008 numbering)
  - Still some work needed to properly tag source text to be able to generate fully correct 1076.1-2007 or 1076-2008 documents
    - See open issue on next slide
- **Remaining work**
  - Generate FM sources for Clauses 10(12) to 15(24)
    - Clauses 17 to 24 are only in P1076-2008
  - Generate FM sources for Annexes A to F(J)
  - Verify clauses and annexes against original LRM documents
  - Generate the indexes

Baseline LRM (2)

- **Open issue: Do we really need to be able to generate fully correct P1076.1-2007 LRM?**
  - Different clause numberings
  - Moved text
  - Placement of Clause 15 (Simultaneous statements) expected in new P1076.1-201X Clause 11 (Architectural statements)
  - If yes, it would require more complicated conditional tag settings
- **Resources**
  - Alain Vachoux, ~6-8h/week
- **Expected timeline**
  - March 2014: FM source of the baseline document
  - April 2014: Verified P1076.1-2007 and P1076-2008 generated LRMs

VHPI-AMS

- **Champion: David Smith**
- **Goal**
  - Extend VHPI data model and definition to include VHDL-AMS objects.
- **Exact status**
  - Initial requirements defined of what will and will not be handled.
  - Acquired an example from Cadence of their VHPI extension.
- **Remaining work**
  - Finish analysis of Cadence extensions.
  - Define the exact objects that are being extended.
  - Update the UML models.
  - Update the C interface package
  - Add description for the LRM
- **Plan to complete work**
  - Resources
    - Initial we had 3. There has been no activity. Currently 1 resource.
  - Time line
    - July for complete of analysis and object definitions.
    - September for the definition of the UML models and C Interface package
    - December for completion of LRM language

1076.1.1 integration

- **Champion: David Smith**
- **Goal**
  - Integrate 1076.1.1 into LRM
  - Add dimension interoperability support (dropped since not essential)
- **Exact status**
  - We defined the tasks with the expectation of an editor. Since the basic integration is an editing task that has been on hold.
- **Remaining work**
  - Rework existing 1076.1.1 text into new 1076.1 LRM.
  - Rework machine readable code to 1076-2008 structure (now distributable).
  - Recommend having this group do the related LRM work to offload Alan.
- **Plan to complete work**
  - Resources
    - We had 2. Done to 1.
  - Time line
    - June for LRM work
    - August for machine readable code.

Mandatory LRM Changes (1)

- **Champion: Ernst Christen**
- **Goals**
  - Update 1076.1-specific definitions to reflect 1076-2008 enhancements
  - Address errata
  - Minor enhancements, e.g. other forms of 'ltf, 'ztf
- **Status**
  - Analyzed integrated document to understand major alignment issues
    - See table
- **Dependencies**
  - Baselined LRM

Mandatory LRM Changes (2)

Task	Duration
Generic natures	4w
Unconstrained, unbounded, fully constrained natures	8w
External names	1w
Support for new operators in • simultaneous if statements • simultaneous case statements • sequential and concurrent break statements	4w
Elaboration	4w
Initialization and simulation cycle (VHPI integration)	6w
Miscellaneous alignments	8w
Errata	4w
Minor enhancements	8w

Mandatory LRM Changes (3)

- **Plan**
  - Generate Language Change Specifications (LCS) for major alignment items, enhancements, errata
    - Identify and document changes by LRM section
    - Review
    - Work with Alain to update LRM
  - Directly edit LRM for minor alignment items
  - Resources
    - Ernst Christen
    - Alain Vachoux
  - Time line
    - Can start when LRM baseline is in advanced state
    - Duration see table

Frequency Domain Modeling

- **Participants**
  - Ernst Christen (champion), Joachim Haase, David Smith, Zhichao Deng, Brian Mulvaney, Subramanian Sivaramakrishnan
- **Goals**
  - Extend language definition to support models whose small-signal frequency domain behavior is defined by a general complex transfer function that is an explicit function of the simulation frequency
- **Status**
  - Investigations and LCS completed
  - Needs approval by Working Group
- **Plan**
  - Review LCS
  - WG approval
  - LRM update

Mixed Netlists

- **Champion: Ernst Christen**
- **Goals**
  - Define semantics for associating formal ports with actuals that are incompatible, e.g. signal and terminal
  - Define rules for inserting instances of conversion models
- **Status**
  - White paper describing a subset of the above goals on twiki
- **Remaining work**
  - Review white paper in light of updated requirements
  - Revise solution based on new requirements
  - Define rules for configuring insertion of conversion module instances
  - Define elaboration rules
- **Plan**
  - Estimated effort is > 1 person year (duration)

Table-Driven Modeling – Organization & Goal

- **Participants in TDM subcommittee activities:**
  - Joachim Haase (champion), Ernst Christen, Arpad Muranyi, Alain Vachoux, David Smith, Thuy Tran, Zhichao Deng
- **Meetings**
  - First meeting June 2, 2010
  - Last meeting September 25, 2012
    http://www.eda.org/twiki/bin/view.cgi/P10761/TDMMtgMinutesSep2512
- **Twiki site**
  http://www.eda.org/twiki/bin/view.cgi/P10761/ProjectTableDrivenModeling
- **Goals given by document**
  Requiremets for Table-Driven Modeling (v1.0 – 2010-11-08)
  http://www.eda.org/twiki/pub/P10761/ProjectTableDrivenModeling/TDM_Requirements.txt

Table-Driven Modeling – Exact Status

- **Test implementation (v0.10 – 2012-05-24)**
  - VHDL-2008 features applied
    (esp. unconstrained arrays in record declarations)
  - Documentation via
    http://www.eda.org/twiki/pub/P10761/ProjectTableDrivenModeling/tdm_v0.10_doc_proposal.pdf
    http://www.eda.org/twiki/pub/P10761/ProjectTableDrivenModeling/tdm_v0.10_doc.pdf
  - Code via
    http://www.eda.org/twiki/pub/P10761/ProjectTableDrivenModeling/tdm_v0.10.zip
    Start of online documentation via doc/index.html
- **Open issues**
  - Hiding in TABLE_INTERPOLATION_PKG the declaration of
    - TABLE_DATA_REAL
    - TABLE_DATA_COMPLEX
  - Declaration of function interfaces to handle [TDM-R14]
    - IBIS files
    - Excel CSV files
  - See minutes draft for the last telco on September 25, 2012
    http://www.eda.org/twiki/bin/view.cgi/P10761/TDMMtgMinutesSep2512

Table-Driven Modeling – Remaining Work

- **Decide on how to handle open issues**
  - Hiding of declarations in the header of TABLE_INTERPOLATION_PKG
  - Interfaces for CSV and Excel files
- **Consideration of feedback to current status**
  - From Alan Coutay (Synopsys) – 2013-05-01 considering
    - Splitting TDM use into preparation and evaluation phase
    - Providing quadratic interpolation
    - Providing different methods for cubic interpolation
    - Handling of complex look-up tables
    - Specific requirements as integral calculation, reduction of dimension, …
- **Update and test of the test implementaion**
- **Update of the documentation for evaluation by the WG**

Table-Driven Modeling – Plan to complete work

- **Resources**
  - Availibility of stable tool for test implementation
- **Time line**
  - Restart of activities 02.2014
    - Recalling status – including feedback
    - Agreement on schedule for further activities
  - Decision on open issues/solution for them 04.2014
  - Completion of test implementation and documentation 06.2014
    - Either based on VHDL-2008
    - Or restricted to VHDL 1076.1-2007
  - Collection of feedback from WG 09.2014
  - Preparation of proposal for standardization 11.2014
- **Expected results**
  - Proposal for standardization
  - Package header for TABLE_INTERPOLATION_PKG

Vector/Matrix Operations (1)

- **Champion: Zhichao Deng**
- **Phase 1.**
  - Establish the "Requirements for matrix/vector support with VHDL-AMS"
  - As a starting point the draft proposal can be used Ref. 1.
- **Phase 2.**
  - Definition of VHDL(-AMS) function headers and standard package header resp.
  - Some aspects can be found in slide 7 of Ref. 2.
- **Phase 3.**
  - Reference implementation of functions and standard package body resp.
- **Phase 4.**
  - Test of the reference implementation

This is the current status

Vector/Matrix Operations (2)

- **Phase 5.**
  - A second round of requirement consolidation with VHDL and possibly SystemVerilog (Verilog) will be started in Jan 2014 and expected completion time is April 2014.
- **Phase 6.**
  - submit the consolidated package and requirement to the VHDL-AMS community for approval. Expected completion time: July 2014.
- **Phase 7.**
  - add the package and corresponding section into VHDL-AMS standard draft. Expected completion time: Sep 2014.
- **Phase 8.**
  - any other final changes about typo and other small things in VHDL-AMS standard. Expected completion time: Nov 2014.
- **Phase 9.**
  - Finishing of documentation - proposal for the standard revision

Next Steps

- **Discussion about project disposition**
  - Coordination with P1076
  - Between WG members first
  - On reflector
- **Define process for LRM updates**
- **Vote by WG**
- **Next meetings (announced at www.eda.org/vhdl-ams):**
  - Wednesday, February 12, 2014, 8:00am PST (15:00 UTC)
  - Wednesday, March 12, 2014, 8:00am PDT (16:00 UTC) (tentative)